WHAT IS CLAIMED IS:

1. For use in a receiver capable of decoding trellis encoded signals, a two stage decision feedback equalizer comprising:

a first stage equalizer comprising a first forward equalizer filter, a first decision feedback equalization filter, and a trellis decoder,

wherein said first decision feedback equalization filter is coupled to each path memory output of said trellis decoder, said first decision feedback equalization filter capable of obtaining symbol values from each path memory output of said trellis decoder for use as an estimate in channel equalization; and

a second stage equalizer coupled to said first stage equalizer, said second stage equalizer comprising a second forward equalizer filter, and a second decision feedback equalization filter,

wherein an input of said second stage decision feedback equalization filter is coupled to an output of said trellis decoder.

2. The two stage decision feedback equalizer as claimed in Claim 1 wherein said second stage equalizer cancels post echoes caused by latency in the feedback path of said first stage equalizer.

3. The two stage decision feedback equalizer as claimed in Claim 1 further comprising a buffer having an output coupled to said second stage equalizer, said buffer capable of receiving an input signal that is provided to an input of said first stage equalizer, said buffer capable of delaying the transfer of said input signal to said second stage equalizer.

4. The two stage decision feedback equalizer as claimed in Claim 3 wherein said second stage equalizer cancels pre-echoes caused by latency in the feedback path of said first stage equalizer.

5. The two stage decision feedback equalizer as claimed in Claim 4 wherein said pre-echoes are cancelled in said second stage equalizer by selecting an amount of delay D in said buffer that causes said pre-echoes to be cancelled.

6. The two stage decision feedback equalizer as claimed in Claim 3 wherein said first stage equalizer cancels pre-echoes caused by latency in the feedback path of said first stage equalizer.

7. For use in a receiver capable of decoding trellis encoded signals, a two stage decision feedback equalizer in which forward filter coefficients, $f^k$, remain constant for the duration of D symbols, said two stage decision feedback equalizer comprising a forward equalizer filter, a first decision feedback equalization filter, a trellis decoder, a delay buffer, and a second decision feedback equalization filter

wherein said first decision feedback equalization filter is coupled to each path memory output of said trellis decoder, said first decision feedback equalization filter capable of obtaining symbol values from each path memory output of said trellis decoder for use as an estimate in channel equalization;

wherein an input of said second stage decision feedback equalization filter is coupled to an output, $a_k$, of said trellis decoder;

wherein an output signal, $B_k$, of said forward equalizer filter is provided to said delay buffer and said delay buffer delays said signal for a duration of D symbols; and

wherein an output signal, $b_k$, of said delay buffer is added to an output signal of said second feedback decision equalization filter to form an output signal, $y_k$, for said two stage decision feedback equalizer.

8. The two stage decision feedback equalizer as claimed in Claim 7 further comprising:

an error unit capable of forming an error signal, $e_k$, from an output, $y_k$, of said two stage decision feedback equalizer, and from an output, $a_k$, of said trellis decoder, and from a signal output from said trellis decoder that represents the number of states identical to the state that produced trellis output $a_k$.

9. The two stage decision feedback equalizer as claimed in Claim 8 wherein said error unit is capable of forming error signal, $e_k$, with one of: a blind error calculation algorithm and a least mean squares calculation algorithm.

10. The two stage decision feedback equalizer as claimed in Claim 7 comprising:

a forward equalizer filter unit comprising said forward equalizer filter;

a trellis decoder; and

a decision feedback equalization filter unit comprising said first decision feedback equalization filter and said second decision feedback equalization filter

wherein said first decision feedback equalization filter is

coupled to each path memory output of said trellis decoder, said first decision feedback equalization filter capable of obtaining symbol values from each path memory output of said trellis decoder for use as an estimate in channel equalization.

11. The two stage decision feedback equalizer as claimed in Claim 10 further comprising a delay unit within a random access memory unit coupled to said forward equalizer filter unit, said delay unit capable of computing a delayed input signal, $r_k$, to said forward equalizer filter unit, from input signal, $R_k$, to said forward equalizer filter unit, from the expression $r_k = R_{k-D}$ where D is a delay of D symbols.

12. The two stage decision feedback equalizer as claimed in Claim 11 wherein said delay unit within said random access memory unit is capable of computing a delayed input signal, $b_k$, from said delay unit from output signal, $B_k$, from said forward equalizer filter unit, from the expression $b_k = B_{k-D}$ where D is a delay of D symbols.

13. The two stage decision feedback equalizer as claimed in Claim 12 wherein said random access memory unit is capable of storing input signals, $r_k$, to said forward equalizer filter unit, and capable of storing output signals, $b_k$, from said delay unit.

14. The two stage decision feedback equalizer as claimed in Claim 11 further comprising:

an error unit capable of forming an error signal, $e_k$, from an output, $y_k$, of said two stage decision feedback equalizer, and from an output, $a_k$, of said trellis decoder, and from a signal output from said trellis decoder that represents the number of states identical to the state that produced trellis output $a_k$.

15. The two stage decision feedback equalizer as claimed in Claim 14 wherein said error unit is capable of forming error signal, $e_k$, with one of: a blind error calculation algorithm and a least mean squares calculation algorithm.

16. A high definition television receiver capable of decoding trellis encoded signals comprising a two stage decision feedback equalizer comprising:

a first stage equalizer comprising a first forward equalizer filter, a first decision feedback equalization filter, and a trellis decoder,

wherein said first decision feedback equalization filter is coupled to each path memory output of said trellis decoder, said first decision feedback equalization filter capable of obtaining symbol values from each path memory output of said trellis decoder for use as an estimate in channel equalization; and

a second stage equalizer coupled to said first stage equalizer, said second stage equalizer comprising a second forward equalizer filter, and a second decision feedback equalization filter,

wherein an input of said second stage decision feedback equalization filter is coupled to an output of said trellis decoder.

17. A high definition television receiver comprising a two stage decision feedback equalizer in which forward filter coefficients, $f^k$, remain constant for the duration of D symbols, said two stage decision feedback equalizer comprising a forward equalizer filter, a first decision feedback equalization filter, a trellis decoder, a delay buffer, and a second decision feedback equalization filter

wherein said first decision feedback equalization filter is coupled to each path memory output of said trellis decoder, said first decision feedback equalization filter capable of obtaining symbol values from each path memory output of said trellis decoder for use as an estimate in channel equalization;

wherein an input of said second stage decision feedback equalization filter is coupled to an output, $a_k$, of said trellis decoder;

wherein an output signal, $B_k$, of said forward equalizer filter is provided to said delay buffer and said delay buffer delays said signal for a duration of D symbols; and

wherein an output signal, $b_k$, of said delay buffer is added to an output signal of said second feedback decision equalization filter to form an output signal, $y_k$, for said two stage decision feedback equalizer.

18. The high definition television receiver as claimed in Claim 17 wherein said two stage decision feedback equalizer comprises:

an error unit capable of forming an error signal, $e_k$, from an output, $y_k$, of said two stage decision feedback equalizer, and from an output, $a_k$, of said trellis decoder, and from a signal output from said trellis decoder that represents the number of states identical to the state that produced trellis output $a_k$.

19. The high definition television receiver as claimed in Claim 18 wherein said two stage decision feedback equalizer comprises:

a forward equalizer filter unit comprising said forward equalizer filter;

a trellis decoder; and

a decision feedback equalization filter unit comprising said first decision feedback equalization filter and said second decision feedback equalization filter

wherein said first decision feedback equalization filter is coupled to each path memory output of said trellis decoder, said first decision feedback equalization filter capable of obtaining symbol values from each path memory output of said trellis decoder for use as an estimate in channel equalization.

20. The high definition television receiver as claimed in Claim 19 wherein said two stage decision feedback equalizer further comprises:

a delay unit within a random access memory unit coupled to said forward equalizer filter unit,

wherein said delay unit is capable of computing a delayed input signal, $r_k$, to said forward equalizer filter unit, from input signal, $R_k$, to said forward equalizer filter unit, from the expression $r_k = R_{k-D}$ where D is a delay of D symbols, and

wherein said delay unit is capable of computing a delayed input signal, $b_k$, from said delay unit from output signal, $B_k$, from said forward equalizer filter unit, from the expression $b_k = B_{k-D}$ where D is a delay of D symbols.

21. For use in a receiver capable of decoding trellis encoded signals, a method for reducing error in a two stage decision feedback equalizer comprising the steps of:

obtaining an estimate of a symbol stream using a first stage equalizer comprising a first forward equalizer filter, a first decision feedback equalization filter, and a trellis decoder; and

providing said estimate of said symbol stream to a second stage equalizer comprising a second forward equalization filter and a second decision feedback equalization filter;

minimizing error is said second stage equalizer using decisions from said trellis decoder.

22. The method as claimed in Claim 21 comprising the step of:

cancelling in said second stage equalizer post echoes that are caused by latency in the feedback path of said first stage equalizer.

23. The method as claimed in Claim 21 comprising the step of:

cancelling in said second stage equalizer pre-echoes that are caused by latency in the feedback path of said first stage equalizer.

24. The method as claimed in Claim 23 wherein said pre-echoes are cancelled in said second stage equalizer by selecting an amount of delay D in a buffer that is capable of delaying the transfer of an input signal to said second stage equalizer, where said selected amount of delay D causes said pre-echoes to be cancelled.

25. The method as claimed in Claim 21 wherein forward filter coefficients, fk, of said first forward equalizer filter and of said second forward equalizer filter remain constant for the duration of D symbols.

26. The method as claimed in Claim 25 further comprising the step of:

forming an error signal, $e_k$, from an output, $y_k$, of said two stage decision feedback equalizer, and from an output, $a_k$, of said trellis decoder, and from a signal output from said trellis decoder that represents the number of states identical to the state that produced trellis output $a_k$.